REMARKS

Applicant appreciates the examination of the present application and the indication that Claims 3, 8-12 and 15 recite allowable subject matter. In response to the initial examination, Applicant has amended page 1 of the specification to fill in the serial number of the domestic priority application. Applicant has also attached hereto a supplemental Declaration and Power of Attorney, which properly identifies the priority application. Claim 4 has also been amended to address the claim objection set forth at page three (3) of the Official Action of June 19, 2003. Thus, the sole outstanding issues are the claim rejections under 35 USC § 102.

All Claims are Patentable Over U.S. Patent No. 5,541,546 to Okumura

Applicant acknowledges that NMOS transistors 302-304 in FIG. 4 of Okumura are configured as diodes. However, the three transistors are configured as a "totem pole" of diodes that provide a constant voltage drop of Vth+Vth+Vth = 3Vth, where Vth is the threshold voltage of the NMOS transistors 302-304. Like the two resistors 201-202 in FIG. 3, the three NMOS transistors 302-304 and resistor 301 in FIG. 4 operate as a voltage divider that maintains node VC at a constant voltage:

> "In this embodiment, the constant voltage supply portion 100 uses the low voltage source terminal V1 directly and, therefore, a potential at the constant voltage terminal VC is equal to a high level potential of a signal input to the input terminal I of the level conversion circuit.
>
> * * * * *
>
> In FIG. 4, it is possible to supply a potential which is a sum of threshold voltages of the enhancement N channel MOS transistors 302, 303 and 304 to the constant voltage terminal VC by setting a resistance value of the resistor 301 considerably larger than resistance values of the diode-connected NMOS transistors 302, 303 and 304.
>
> Although, in FIG. 4, the number of the diode-

> connected NMOS transistors is three, the number can be suitable selected. In this case, the potential of the constant voltage terminal VC must be higher than a sum of the low level potential VL of the input terminal I shown in FIG. 1 and the threshold voltage VT of the enhancement N channel MOS transistor 107 and lower than a sum of the high level potential VH of the input terminal I and the threshold voltage VT of the enhancement N channel MOS transistor 107, as described with respect to FIG. 3."

(Okumura, Col. 6, lines 19-24 and Col. 9, lines 32-48).

In stark contrast to the use of a constant voltage VC supplied by three series-connected diodes in FIG. 4 of Okumura, the voltage at the gate of transistor T3 in FIG. 3B of the present application is capacitively bootstrapped to the input voltage (Vin) and varies between a high level of $Vdd2+Vth_{(T2)}$ and a low level of $Vdd2-Vth_{(T1)}$. This variation in the voltage at the gate of transistor T3 is best illustrated by the waveform $V_{GATE-T3}$ in FIG. 4 of the application.

The variation in voltage is supported by two diodes T1 and T2 in FIG. 3B of the present application. These diodes T1 and T2 are not connected in series. Instead, as illustrated by FIG. 3B and Exhibit A (attached hereto), these diodes T1 and T2 are connected antiparallel (anode-to-cathode and cathode-to-anode), as described at page 10, lines 5-14 of the present application.

Thus, it cannot be reasonably maintained that Okumura discloses or suggests "a voltage clamping circuit comprising first and second diodes electrically connected in antiparallel between a power supply line and a gate of said pass transistor", as recited by Claim 1. Moreover, Okumura does not disclose or suggest a "voltage clamping circuit that is ... configured to dynamically clamp a capacitively bootstrapped variable voltage at the gate of said pass transistor", as recited by Claim 4. Instead, in FIG. 1 of Okumura, the voltage VC at the gate of NMOS transistor 107 is constant (see, FIG. 4), not variable. The variable nature of the voltage provided to the gate of NMOS transistor T3 in FIG. 3B of the present application, which is illustrated by a waveform in FIG. 4, precludes an

excessive voltage from appearing across any two terminals of transistor T3 when VIN=2Vdd. These same arguments also apply to independent Claims 13 and 20 of the present application.

Applicant has shown that Okumura manifestly does not disclose or suggest the voltage clamping circuit illustrated and described by the present application and recited by the claims. Moreover, Okumura does not disclose or suggest the capacitively bootstrapped clamping functions performed by the claimed voltage clamping circuit which, as illustrated by FIG. 4 of the present application, causes the variable voltage at the gate of transistor T3 to swing between two voltage levels (Vdd+Vth (high) to Vdd-Vth (low)).

Based on these amendments and remarks, Applicant respectfully submits that the present application is in condition for allowance. The Examiner is encouraged to contact the undersigned by telephone in the event any outstanding issues remain that may prevent issuance of the present application.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on September 29, 2003.

Candi L. Riggs
Date of Signature: September 29, 2003

SUBSTITUTE DECLARATION AND POWER OF ATTORNEY

Attorney Docket No. 5646-54 (IDT Ref. 1634)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **OVERVOLTAGE PROTECTION CIRCUITS,**

the specification of which

☐ is attached hereto

OR

☒ was filed on June 26, 2001 as United States Application No. 09/891,906.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37 Code of Federal Regulations, §1.56, including material information that became available between the filing date of the prior application and the National or PCT International filing date of the continuation-in-part application, if applicable.

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below.

60/298,668	06/15/2001
Application Number(s)	Filing Date (MM/DD/YYYY)
Application Number(s)	Filing Date (MM/DD/YYYY)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

SUBSTITUTE DECLARATION AND POWER OF ATTORNEY - CONTINUED

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following registered attorney(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. I also appoint the following registered attorney(s) to represent me before all competent International Authorities in connection with any and all international applications filed by me with an appropriate receiving office claiming priority to the U.S. application. I also appoint the following registered attorney(s) to make or receive payment on my behalf in connection with the filing of such international applications.

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